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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,673	02/06/2004	Gerald George Pechanek	800.0141	7530

73846 7590 10/09/2007

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
10/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,673	PECHANEK ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 9-26 have been examined; Claims 1-8 have been cancelled.

Acknowledgment of papers filed: amendments and remarks filed on 21 August 2006. The papers filed have been placed on record.

Specification

2. The title is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

1. Objections are withdrawn.

Claim Rejections - 35 USC § 112

2. Rejection is withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371 (c) of this title before the invention thereof by the applicant for patent.

4. Claims 9, and 18-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Sheaffer (U.S. Patent No. 6,957,321).

5. Regarding claim 9, Sheaffer discloses a very long instruction word memory system (col 5 lines 48-51) comprising: a VLIW memory having a plurality of instruction slots for storing instruction words at addressable locations in the VLIW memory form which VLIWs may be fetched for execution (col 7 lines 1-3); said plurality of instruction slots comprising standard width instruction slots for storing standard width instructions and at least expanded width instruction slot having a width that is greater than the standard width instruction slots, the expanded with instruction slot used for storing an expanded width instruction having a format that is wider than the standard with instructions (col 1 lines 33-50 or col 2 line 65 to col 3 line 7);

Note that either method could be viewed as an expanded format.

The VLIW memory configured for loading said at least one expanded format slot with an expanded instruction (col 7 lines 1-3).

Note the term "fetched" is considered to suggest loading an instruction.

6. Regarding claim 18, Sheaffer discloses a very long instruction word (VLIW) memory system (col 5 lines 48-51) comprising: an instruction memory holding a plurality of instructions of a first bit width , the plurality of instructions having at least one execute VLIW instruction; and a very long instruction memory having instruction slots for storing instructions of a second bit width different from the first vit width and wherein the very

long instruction memory hodls VLIWs at addressable locations that may be fetched as a result of executing the at least one execute VLIW instruction (col 1 lines 33-50 or col 2 line 65 to col 3 line 7).

Note that in the first citation, the instruction with prefix and escape codes is considered to be the wide format. In the second citation, the instruction, with the additional NOP extensions, is considered to be the wide format. Although the prefix/escape codes are discussed in the background, they can be implemented with the present referenced invention, as indicated in col 7 lines 64-67.

7. Regarding claim 19, Sheaffer discloses the system of claim 18 wherein instructions of the second bit width are stored in a data memory and delivered to the very long instruction memory utilizing a data bus (col 5 lines 48-51 and col 7 lines 1-3 and fig 4 reference 410).

8. Regarding claim 20, Sheaffer discloses a very long instruction word (VLIW) memory system comprising: a plurality of instruction slots for storing instruction words forming a VLIW (col 5 lines 48-51), at least one of said plurality of instruction slots having a compressed format for storing a compressed instruction having a narrower instruction format with respect to an instruction format required in a program storage wherein the VLIW resides at an addressable location in a VLIW memory, the VLIW memory holding VLIWs that may be fetched for execution (col 1 lines 33-50 or col 2 line 65 to col 3 line 7);

Note that on paragraph 53 of Applicant's specification, the instructions designated as "compressed instructions" appear to be essentially the same as the extended instructions, just through a different view point. As claimed (in light of the Applicant's specification), it appears reasonable to consider the non-extended instruction a compressed instruction.

And means for loading said at least one compressed format slot with a compressed instruction (see below).

Note that the "compressed format" is considered to be a regular instruction without any escape bits, preflix bits, or NOP operands.

9. Regarding claim 21, Sheaffer discloses a processing apparatus comprising: a memory for storing a processing apparatus program comprising short instruction words (col 7 lines 1-3); an indirect very long instruction word (VLIW) memory comprising a plurality of instruction slots for storing instruction words (col 5 lines 48-51 and col 7 lines 1-3),

Note that the term "indirect" appears to be referring to an "indirect execution mechanism" in Applicant's specification. This mechanism is anticipated by the additional NOP operands that are indirectly used in execution.

At least one of said instruction slots having an instruction format sized according to execution function and operand storage capacity (col 3 lines 1-7)

Note that, clearly, the instruction slot is going to be sized based on the execution function (the size requirement for the execution units) and the operand storage capacity (the necessary bits required for the operand)

And independent of the size of the short instruction words , wherein the plurality of instruction slots are organized to form a plurality of VLIWs and each VLIW resides at an addressable location in the indirect VLIW memory, the indirect VLIW memory holding VLIWs that may be fetched for execution (col 3 lines 1-7);

Note that the use of prefix/escape and NOP expansions indicates that the format is sized independent of the short instruction word size.

At least one data memory unit storing instruction operands (fig 4); and at least two execution units for executing a VLIW fetched from the indirect VLIW memory (col 6 lines 35-36) in response to a short instruction word dispatched from the memory (see below).

Note that the VLIW instruction is comprised of several short instruction words, indicating that the execution units will execute the VLIW instruction words in response to a short instruction word.

10. Regarding claim 22, Sheaffer discloses the processing apparatus of claim 21 wherein the short instruction words comprise K-bits (fig 5) and the instruction format comprises T-bits, wherein T.noteq.K (col 3 lines 1-7).

Note that the short instruction words have a different number of bits than the instruction slot, the slot considered to hold the additional bits in the extensions for either escape/prefix codes or NOP operands.

11. Regarding claim 23, Sheaffer discloses the processing apparatus of claim 22 wherein the instruction format comprises at least one operand address field of B-bits supporting direct operand addressing (fig 4a reference 515).

12. Regarding claim 24, Sheaffer discloses the processing apparatus of claim 23 wherein the data memory unit has a capacity 2.sup.B data values (see below).

Note that it is clearly implied that there are 2^B data values. That is the whole point of having B bits in an address.

13. Regarding claim 25, Sheaffer discloses the processing apparatus of claim 21 wherein a at least one of the at least two execution units operate on a slot instruction format and directly access operands from the data memory unit for execution (fig 5 and col 3 lines 1-7).

Note that the instructions do not necessarily have to contain any extensions. They can just be regular instructions. Consequently, the execution units can directly access operands from the data memory unit for execution. Additionally, as shown in fig 5, some operands are accessed directly even when an NOP instruction extension takes place.

14. Regarding claim 26, Sheaffer discloses the processing apparatus of claim 21 wherein the at least two execution units operate as two execution units (col 6 lines 35-36)

When executing two VLIW memory slot instructions as specified by a two slot execute VLIW instruction (fig 5 and col 5 lines 49-51),

Note that an XV instruction (which appears to be an execute VLIW instruction in Applicant's specification) is considered to be a VLIW instruction executed in the processor or, essentially, a typical VLIW instruction.

And wherein the at least two execution units operate as one execution unit when executing one VLIW memory slot instruction as specified by a one slot execute VLIW instruction (col 3 lines 1-7).

Note that VLIW instructions can take up a varying number of slots, depending on how the compiler combines the short instructions into VLIW instructions. Consequently, the execution unit executes the VLIW instructions no matter what number of "slots" are occupied by this instruction.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 10, 11, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheaffer in view of Moller (U.S. Patent No. 6,826,522).

17. Regarding claim 10, Sheaffer discloses the memory system of claim 9 wherein the plurality of instruction slots comprise a store unit instruction slot (col 9 lines 13-19), a load unit instruction slot (col 9 lines 13-19),

Note that the storing of instructions clearly implies the necessity of a loading unit as well, otherwise the stored instructions could not be accessed and no interesting program would be able to run on this processing unit.

An arithmetic logic unit (ALU) instruction slot (col 9 lines 14-15), and a data store unit (DSU) instruction slot (col 9 lines 13-19).

Sheaffer fails to disclose a multiply accumulate unit instruction slot.

Moller discloses a multiply accumulate instruction unit (col 5 lines 11-12)

Sheaffer, a computer system that already contains an arithmetic logic unit, would likely be motivated to include instructions that provide further flexibility to the programmer. A multiply accumulate instruction is well known in the art and allows the programmer to complete varies applications in one instruction, rather than two—making the system less complicated and often faster. For these reasons, Sheaffer would be motivated to include a multiply accumulate instruction.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the computing system of Sheaffer and include the multiply accumulate

instruction/unit of Moller. Clearly, as this instruction is incorporated, instruction slots would be available to save a MAC instruction in instruction memory.

18. Regarding claim 11, Sheaffer discloses the memory system of claim 10 wherein the store unit instruction slot is an expanded width instruction slot that stores an expanded width store instruction including additional bits to extend compute register fiele addressing, an additional bit to extend address register file addressing (col 3 lines 16-19), an additional bit to expand an opcode file, or an additional bit to extend a conditional field.

Note that the "or clause" of the claim requires only one limitation to be anticipated.

19. Regarding claim 13, Sheaffer discloses the memory system of claim 10 where the load unit instruction slot is an expanded width instruction slot that stores an expanded width load instruction of a first format for load immediate operations including additional bits to extend compute register file addressing, a bit to extend address file register addressing (col 3 lines 16-19 and col 9 lines 13-19),

Note, in the second citation, that the result is stored in a double-wide register. Since this is treated as one register, this would suggest that loading would work the same way, extending the register addressing.

A bit to extend a conditional field or sixteen bits to extend an immediate field.

Note that, again, the "or clause" of the claim requires only one limitation to be anticipated.

20. Regarding claim 15, Sheaffer discloses the memory system of claim 10 where the ALU, MAU and DSU instruction slots are expanded width instruction slots that store expanded width ALUE, MAU, and DSU instructions including additional bits in each operand field to extend compute register file addressing (col 9 lines 13-19), a bit to extend an opcode field, or a bit to extend a data type field.

21. Claims 12, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheaffer/Moller in view of Tremblay (U.S. Patent No. 6,341,348).

22. Regarding claim 12, Sheaffer discloses the memory system of claim 11. wherein said expanded with store instruction supports expansion of a 32.times.32 bit/16.times.64 bit configurable register file (103 with Tremblay) size to a 128.times.32 bit/64.times.64 bit/32.times.128 bit configurable register file size.

Sheaffer/Moller fails to disclose a register file of size 128.times.32 bit/64.times.64 bit/32.times128 bit.

Tremblay discloses a register file with 128 32-bit registers (col 5 lines 39-41).

Sheaffer/ Moller fails to disclose the size of its register file. Sheaffer/Moller would likely be motivated to utilize a similar size as another VLIW invention (Tremblay col 5 line 57). Clearly, the size of the register file depends on particular aspects of the

invention not necessarily disclosed in a patent attributed to a specific feature. Sheaffer/Moller would have been reasonably motivated to utilize a register file of any reasonable size.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the invention of Sheaffer/Moller and incorporate a register file with 128 32-bit registers. Sheaffer also discloses the technique of grouping registers into pairs and quads (col 1 line 66 to col 2 line 8), allowing for a register file with 64 64 bit registers and 32 128 bit registers.

Note that it is unclear how the claimed register file is being expanded. This claim appears to be simply claiming a register file of the larger size given.

23. Regarding claim 14, Sheaffer discloses the memory system of claim 13 wherein said expanded with load instruction supports expansion of a 32.times.32 bit/16.times.64 bit configurable register file size to a 128.times.32 bit/64.times.64 bit/32.times.128 bit configurable register file size (Tremblay col 5 lines 39-41 and Sheaffer col 1 line 66 to col 2 line 7--see claim 12).

24. Regarding claim 16, Sheaffer discloses the memory system of claim 15 wherein said expanded width ALU, MAU, and DSU instructions each supports expansion of a 32.times.32 bit/16.times.64 bit configurable register file size to a 128.times.32 bit/64.times.64 bit/32.times.128 bit configurable register file size (Tremblay col 5 lines 39-41 and Sheaffer col 1 line 66 to col 2 line 7--see claim 12).

25. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sheaffer in view of Pechanek (U.S. Patent No. 6,173,389).

26. Regarding claim 17, Sheaffer discloses a very long instruction word (VLIW) instruction (col 5 lines 48-51) memory (VIM) basket (VIMB) (col 7 lines 1-3)

Note that it is unclear what is meant by the term "memory basket". A basket is a device used to place items for later use, so a VLIW basket would appear to be a place to store VLIW instructions, namely an instruction memory.

an instruction bit organizer for receiving instructions as data and organizing the bits from the data encoded instructions into proper format for loading into the VIMB (see below);

And the VIMB comprising a plurality of instruction slots having expanded instruction slot width greater than the width of the instruction format required in program storage (col 1 lines 33-50 or col 2 line 65 to col 3 line 7).

Sheaffer fails to disclose a load indirect instruction or a mask bit field specifying which slots will be loaded in a VLIW having at least one instruction slot that is an expanded instruction slot, the VLIW accessible to be loaded at an addressable location into the VIMB.

Pechanek discloses a load indirect instruction and a load mask bit field (col 3 lines 24-33).

The technique in Pechanek is advantageous to utilize hardware more efficiently and reduce duplicate instructions (col 2 lines 12-27)

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Sheaffer and incorporate the indirect instruction with load mask bit field of Pechanek.

Response to Arguments

27. Applicant's arguments filed 21 August 2006 have been fully considered but they are not persuasive.

28. Appellant states:

"Both an existing instruction and its associated operand bearing NOP instruction must be decoded together before the benefits of the operand bearing NOP instruction can be obtained...In contrast to Sheaffer, the present invention does not require a decoder, such as Sheaffer's decoder 205, to translate from one instruction set to another instruction set As recited in amended claim 9, VLIWs, made up of the instruction slots, are stored 'at addressable locations in a VLIW memory form which VLIWs may be fetched for execution"

Applicant appears to argue that the "expanded VLIW instruction" as view by Examiner is, in reality, two separate instructions and, therefore, does not satisfy the claim limitations. Examiner disagrees.

Examiner directs Applicant's attention to col 5 lines 5-15 of Sheaffer:

"Some instruction sets include variable length instructions. Often such instruction sets are considered 'complex' and the computers designed around such complex instruction sets are referred as a Complex Instruction Set Computer (CISC) architecture computers. On the other hand, there are also Reduced Instruction Set Computers (RISC) architecture machines. Such machines generally use simpler and smaller instruction sets to accomplish the same tasks by using larger numbers of such instructions (i.e., software becomes more complex). It is expressly understood that the inventive features of the present disclosure may be usefully embodied in a number of alternative processor architectures that will benefit from the techniques disclosed."

It is clear from this disclosure that the first instruction and operand specifying NOP instruction can be appropriately characterized as a variable length instruction. This interpretation is supported by the fact that this/these instruction(s) are simultaneously fetched from memory and shown in contiguous locations on Fig. 2A (indicating a single memory location).

Appellant claims that the decoder 205 of Sheaffer is not required by Applicant's invention. If this is the case, this distinction needs to be made clear within the claim language for Examiner to give it patentable weight.

29. Applicant's argument with respect to claim 18 appears to hinge on the same detail as shown above, the fact that the two instructions of fig. 2a and 2b cannot be characterized as a single instruction. As indicated with respect to claim 9, Examiner disgrees.

30. Applicant's arguments with respect to claim 17 are moot in view of a new grounds rejection.

31. Examiner further notes that Applicant has failed to address with respect to many claims the interpretation resulting from the prefix bits shown in col 1 lines 33-43.

Conclusion

32. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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